Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1-16 (Canceled).

17. (Previously presented) A system comprising:

a voltage monitor to monitor a voltage of the system and to transmit a voltage monitor signal if the voltage falls below a predetermined threshold;

a power delay circuit to transmit a power delay signal in response to receiving a voltage monitor signal and to transmit a reset signal if the voltage monitor signal indicates a reset condition or in response to an external event reset signal;

a memory sub-system to store digital data and having a self-refresh circuit, the self-refresh circuit causing the memory sub-system to enter into a self-refresh sequence; and

a memory controller to control and configure the memory sub-system, the memory controller having a power fail controller to receive a power delay signal or a reset signal from the power delay circuit, the power controller asserting a system reset signal and sending two configuration signals in response to the power delay signal or external event reset signal, the configuration signals indicating whether the external event reset signal was detected for at least a predetermined amount of time and at least one of a power failure or an external reset event is detected.

18. (Previously presented) The system of claim 17, wherein the memory controller further comprises a state machine to receive the system reset signal and the configuration signals and to direct the memory sub-system into a self-refresh state based on the system reset signal and the configuration signals.

19. (Previously presented) The system of claim 17, further comprising means for generating an external event signal.

20. (Previously presented) The system of claim 17, wherein the power fail controller prevents the self-refresh sequence from executing when the system is not configured.

21. (Canceled).

22. (New) A system comprising:

a voltage monitor to monitor a voltage of the system and to transmit a voltage monitor signal if the voltage falls below a predetermined threshold;

means for transmitting a power delay signal and a reset signal, wherein the power delay signal is transmitted in response to receiving a voltage monitor signal and the reset signal is transmitted if the voltage monitor signal indicates a reset condition or in response to an external event reset signal;

a memory sub-system to store digital data and having a self-refresh circuit, the self-refresh circuit causing the memory sub-system to enter into a self-refresh sequence; and

a memory controller to control and configure the memory sub-system, the memory controller having a power fail controller to receive a power delay signal or a reset signal from the means for transmitting a power delay signal and a reset signal, the power controller asserting a system reset signal and sending two configuration signals in response to the power delay signal or external event reset signal, the configuration signals indicating whether the external event reset signal was detected

for at least a predetermined amount of time and at least one of a power failure or an external reset event is detected.

23. (New) The system of claim 22, wherein the memory controller further comprises a state machine to receive the system reset signal and the configuration signals and to direct the memory sub-system into a self-refresh state based on the system reset signal and the configuration signals.

24. (New) The system of claim 22, further comprising means for generating an external event signal.

25. (New) The system of claim 22, wherein the power fail controller prevents the self-refresh sequence from executing when the system is not configured.

26. (New) A system comprising:

means for monitoring a voltage of the system and to transmit a voltage monitor signal if the voltage falls below a predetermined threshold;

a power delay circuit to transmit a power delay signal in response to receiving a voltage monitor signal and to transmit a reset signal if the voltage monitor signal indicates

a reset condition or in response to an external event reset signal;

a memory sub-system to store digital data and having a self-refresh circuit, the self-refresh circuit causing the memory sub-system to enter into a self-refresh sequence; and

means for controlling and configuring the memory sub-system, the means for controlling and configuring the memory sub-system having a power fail controller to receive a power delay signal or a reset signal from the power delay circuit, the power controller asserting a system reset signal and sending two configuration signals in response to the power delay signal or external event reset signal, the configuration signals indicating whether the external event reset signal was detected for at least a predetermined amount of time and at least one of a power failure or an external reset event is detected.

27. (New) The system of claim 26, wherein the means for controlling and configuring the memory sub-system further comprises a state machine to receive the system reset signal and the configuration signals and to direct the memory sub-system into a self-refresh state based on the system reset signal and the configuration signals.

28. (New) The system of claim 26, further comprising means for generating an external event signal.

29. (New) The system of claim 26, wherein the power fail controller prevents the self-refresh sequence from executing when the system is not configured.